REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-22 are presently active in this case. The present Amendment amends Claims 1, 6-8, 11, 12, 14, and 16-20. New Claims 21 and 22 have been added. Support for new Claims 21 and 22 can be found at least at pages 9, 10 and 19 of the specification. No new matter has been added.

In the outstanding Office Action, Claims 1-5 and 19-20 were rejected under 35 U.S.C. § 102(e) as anticipated by Masui (U.S. Patent No. 6,687,206), and Claims 6-18 were indicated as allowable if rewritten in independent form.

Applicants acknowledge with appreciation the indication of allowable subject matter.

In light of the outstanding rejection based on Masui. Applicants have amended Claims 1, 19, and 20 to recite features of allowable claims and added new Claims 21 and 22 which recite similar features.

Specifically, amended independent Claims 1, 19, and 20 and new Claims 21, and 22 recite, *inter alia*:

> ...an address register configured to latch the address information in synchronization with the prepit clock; and a decoder configured to generate the phase characteristic from the latched address information.

Masui describes a controller that includes an interface circuit which provides a PC interface between the information recording apparatus and an external data processing device, such as a host computer.[1]

However, Masui fails to disclose "an address register configured to latch the address information in synchronization with the prepit clock; and a decoder configured to generate the phase characteristic from the latched address information" as recited in independent

[1] Masui at Column 13, line 67 to Column 14, line 4.

Claims 1, 19, 20, 21, and 22. Furthermore, the Office Action acknowledges that this feature is not found in Masui.[2]

In contrast, Masui describes a data encoder that operates on the write clock signal "Swck" during the writing. The data encoder receives source writing data delivered by the controller, and executes an error correcting code (ECC) process, an 8/16 modulation process and an interleaving process so that the received data is converted into the sequence of recording pulses "Wdata." The data encoder starts outputting the sequence of the recording pulses "Wdata" to the laser driver in response to a write-position start signal "Swps."[3]

Masui, however, fails to teach or suggest a decoder configured to generate the phase characteristic from the latched address information, as recited in Applicants' independent Claims 1, 19, 20, 21, and 22. Thus, Masui does not teach or suggest an address register configured to latch the address information in synchronization with the prepit clock and a decoder configured to generate the phase characteristic from the latched address information as claimed.

Accordingly, Applicants respectfully request that the rejection of Claims 1-5 and 19-20 under 35 U.S.C. § 102(e) be withdrawn.

Consequently, in view of the present amendment, no further issues are believed to be outstanding in the present application, and the present application is believed to be in condition for formal Allowance. A Notice of Allowance for Claims 1-22 is earnestly solicited.

[2] Office Action at Page 5.
[3] Masui at Column 14, line 32 to Column 14, line 40.

Respectfully submitted,

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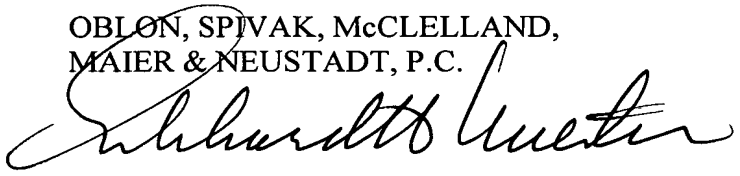

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